REMARKS

This Amendment and Response is filed in reply to the Office action dated October 10, 2006. Claims 1, 3-4, 10-11, 15, 18, 25, 27-28, 38, 50, 53, 55-57, 64, 66, 68-69, 75, 77, 80-81, 83 and 99 are amended, and claims 2, 26, 52, 65 and 70 are canceled. Accordingly, after entry of this Amendment and Response, claims 1, 3-25, 27-51, 53-64, 66-69 and 71-102 remain pending.

I. Claim Rejections Under 35 U.S.C. § 102

Claims 1-102 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,487,639 to Lipasti (hereinafter "Lipasti"). An anticipation rejection requires that each and every limitation of a claim be disclosed in a single prior art reference.

Initially, the rejection of independent claims 1, 25, 38, 50, 64, 68, 83 and 99 is addressed. Independent claim 1 is amended to include the limitation "the processor value predicting for those instances of read operations with values that are unavailable in a low-latency memory and requested from a high-latency memory while ignoring those instances of read operations unavailable in the low-latency memory requested from a second low-latency memory." That is, claim 1 requires predicting values of read operations that miss in a low-latency memory and are requested from a high-latency memory. One advantage of this is that it allows for reduction in the size of the value predictor structure (and processor real estate) by only storing predictions for those read operations incurring large access latencies that significantly impact processor performance. For example, the latency for a miss of a L3 cache (one form of high latency memory) is hundreds of processor clock cycles versus a few to tens of clock cycles for L1 or L2 cache miss (two example forms of low latency memory). Lipasti does not disclose such a limitation.

In contrast to the invention defined by claim 1, Lipasti discloses value prediction of load instructions that miss the data cache (*see Lipasti* column 3, lines 22-25). That is, Lipasti stores predictions for all loads that miss the data cache, and not just those loads that are requested from a high latency memory as required by independent claim 1. Further, the circuit arrangement of Lipasti operates in parallel with a L1 data cache such that predicted values from a L2 cache are provided when a L1 data cache miss occurs (*see Lipasti* column 5, line 62 to column 6, line 2). It is respectfully asserted that L2 cache misses only incur latencies of tens of clock cycles whether the L2 cache is implemented in the processor or off the processor. Thus, Lipasti does not disclose value prediction for low-latency memory misses that are requested from high-latency memory while ignoring those instances of real operations unavailable in the low-latency memory requested from a second low latency memory as required by independent claim 1. Insofar as Lipasti does not disclose all the limitations of independent claim 1, it cannot anticipate independent claim 1.

The other independent claims also include similar limitations of value prediction for read operations that miss in a low-latency memory and are requested from a high-latency memory. Thus, it is respectfully submitted that independent claims 1, 25, 38, 50, 64, 68, 83 and 99 are patentable over Lipasti for at least the above reasons and such indication is respectfully requested.

The remaining rejected claims 3-24, 27-37, 39-49, 51, 53-63, 66-67, 69, 71-82, 84-98 and 100-102 all depend, either directly or indirectly, from one of independent claims 1, 25, 38, 50, 64, 68, 83 and 99. Accordingly, these dependent claims are themselves patentable over Lipasti for at least the reasons set forth above and such indication is respectfully requested. This statement is made without reference to or waiving the independent bases of patentability within each dependent claim.

II. Conclusion

The Applicant thanks the Examiner for his thorough review of the application. The Applicant respectfully submits the present application, as amended, is in condition for allowance and respectfully requests the issuance of a Notice of Allowability as soon as practicable.

This Amendment is submitted contemporaneously with a petition for a one-month extension of time in accordance with 37 C.F.R. § 1.136(a). Accordingly, please charge Deposit Account No. 04-1415 in the amount of $120.00, for a one-month extension of time fee. The Applicant believes no further fees or petitions are required. However, if any such petitions or fees are necessary, please consider this a request therefor and authorization to charge Deposit Account No. 04-1415 accordingly.

If the Examiner should require any additional information or amendment, please contact the undersigned attorney.

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